19-3801; Rev 2; 1/06

±15kV ESD-Protected USB Transceivers with External/Internal Pullup Resistors

General Description

The MAX13481E/MAX13482E/MAX13483E ±15kV ESD-protected USB-compliant transceivers interface low-voltage ASICs with USB devices. The transceivers fully comply to USB 2.0 when operating at full-speed (12Mbps). The transceivers also operate with V_L as low as 1.6V, ensuring compatibility with low-voltage ASICs.

The MAX13481E/MAX13482E/MAX13483E feature a logic-selectable suspend mode that reduces current consumption. Integrated ±15kV ESD circuitry protects D+ and D- bus connections.

The MAX13481E/MAX13482E/MAX13483E operate over the extended -40°C to +85°C temperature range and are available in a 16-pin (3mm x 3mm) thin QFN package.

Applications

Cell Phones

PDAs

Digital Still Cameras

Features

- **Active-Low Enumeration Input Controls D+ Pullup Resistor (MAX13482E)**
- **Active-Low Enumeration Input Controls Internal Pullup Switch (MAX13481E)**
- **±15kV ESD Protection on D+ and D-**
- **USB 2.0 Full-Speed Compliant Transceiver**
- **V_{BUS} Detection (MAX13482E/MAX13483E)**
- **+1.60V to +3.6V V_L Allows Connection with Low-Voltage ASICs**
- **No Power-Supply Sequencing Required**
- **Pin Compatible with MIC2551A (MAX13481E)**
- **Pin Compatible with DP1680 (MAX13483E)**
- **Pin Compatible with DP1681 (MAX13481E)**
- **Pin Compatible with DP1682 (MAX13482E)**

Selector Guide

PART	$\overline{ENUM}$ INPUT	INTERNAL 1.5kΩ RESISTOR	V_{BUS} DETECTION
MAX13481EETE	✓	—	—
MAX13482EETE	✓	✓	✓
MAX13483EETE	—	—	✓

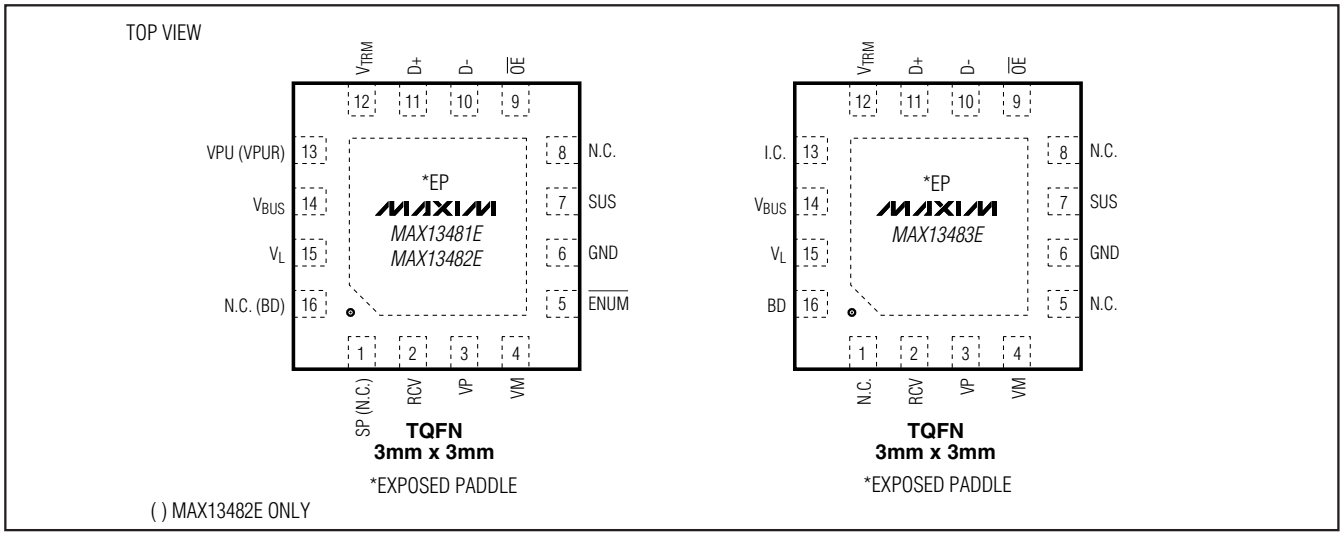
Typical Operating Circuits appear at end of data sheet.

Ordering Information

PART	PIN-PACKAGE	TOP MARK	PKG CODE
MAX13481EETE	3mm X 3mm TQFN-EP*	ADF	T1633-4
MAX13482EETE	3mm X 3mm TQFN-EP*	ADI	T1633-4
MAX13483EETE	3mm X 3mm TQFN-EP*	ADJ	T1633-4

**EP = Exposed Paddle.*

Pin Configurations



±15kV ESD-Protected USB Transceivers with External/Internal Pullup Resistors

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
V_{BUS}, V_L, ...-0.3V to +7V
V_{TRM}, VPUR, VPU.....-0.3V to (V_{BUS} + 0.3V)
Input Voltage (D+, D-).....-0.3V to +7V
VM, VP, SUS, RCV, $\overline{ENUM}$, BD, $\overline{OE}$, ...-0.3V to (V_L + 0.3V)
Short-Circuit Current to V_{CC} or GND (D+, D-)… ..... ±150mA
Maximum Continuous Current (all other pins).....±15mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin, 3mm x 3mm TQFN (derate 15.6mW/°C above +70°C).....1250mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4V to +5.5V, V_L = +1.6V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +2.5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY INPUTS (V_{BUS}, V_{TRM}, V_L)							
V_{BUS} Input Range	V_{BUS}			4.0		5.5	V
V_L Input Range	V_L			1.6		3.6	V
Regulated Supply-Voltage Output	V_{VTRM}			3.0	3.3	3.6	V
Operating V_{CC} Supply Current	I_{VCC}	Full-speed transmitting/receiving at 12Mbps, C_L = 50pF on D+ and D- (Note 2)				10	mA
Operating V_L Supply Current	I_{VL}	Full-speed transmitting/receiving at 12Mbps, C_L = 15pF receiver outputs, V_L = 2.5V (Note 2)				2.5	mA
Full-Speed Idle and SE0 Supply Current	$I_{VCC(IDLE)}$	Full-speed idle, V_{D+} > 2.7V, V_{D-} < 0.3V			250	350	µA
		SE0: V_{D+} < 0.3V, V_{D-} < 0.3V			250	350	
Static V_L Supply Current	$I_{VL(STATIC)}$	Full-speed idle, SE0 or suspend mode				5	µA
Suspend Supply Current	$I_{VCC(SUSP)}$	VM = VP = open, $\overline{ENUM}$ = SUS = $\overline{OE}$ = high				35	µA
Disabled-Mode Supply Current	$I_{VCC(DIS)}$	V_L = GND or open				20	µA
Sharing-Mode V_L Supply Current	$I_{VL(SHARING)}$	V_{BUS} = GND or open, $\overline{OE}$ = low, VP = low or high, VM = low or high, SUS = high, $\overline{ENUM}$ = high				5	µA
Disable-Mode Load Current on D+ and D-	$I_{DX(DISABLE)}$	V_L = GND or open, $V_{D\_}$ = 0 or 5.5V				5	µA
Sharing-Mode Load Current on D+ and D-	$I_{DX(SHARING)}$	V_{BUS} = GND or open, $V_{D\_}$ = 0 or 5.5V				20	µA
USB Power-Supply Detection Threshold	V_{TH_H}	Supply present		3.6			V
	V_{TH_L}	Supply lost	V_L ≥ 1.7V			0.8	
			V_L < 1.7V			0.7	
USB Power-Supply Detection Hysteresis	V_{HYST}				75		mV
V_L Supply-Voltage Detection Threshold	$V_{TH(VL)}$				0.85		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4V to +5.5V, V_L = +1.6V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +2.5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG VOLTAGE OUTPUTS (VPU, VPUR)						
Off-State Leakage	I_{LZ}	$\overline{ENUM}$ = V_L	-1		+1	µA
VPU Switch Resistance		MAX13481E		10		Ω
VPUR Pullup Resistance		MAX13482 (Note 3)	1.425		1.575	kΩ
DIGITAL INPUTS/OUTPUTS (VP,VM, RCV, $\overline{OE}$, $\overline{ENUM}$, SUS, BD)						
Input-High Voltage	V_{IH}	VP, VM, $\overline{OE}$, $\overline{ENUM}$, SUS	0.7 x V_L			V
Input-Low Voltage	V_{IL}	VP, VM, $\overline{OE}$, $\overline{ENUM}$, SUS			0.3 x V_L	V
Output Voltage High	V_{OH}	VP, VM, RCV, BD, I_{SOURCE} = 2mA	V_L - 0.4			V
Output Voltage Low	V_{OL}	VP, VM, RCV, BD, I_{SINK} = 2mA			0.4	V
Input Leakage Current	I_{LKG}		-1		+1	µA
Input Capacitance		Measured from input to GND		10		pF
ANALOG INPUT/OUTPUTS (D+, D-)						
Differential Input Sensitivity	V_{DI}	$\lvert(V_{D+} - V_{D-})\rvert$	200			mV
Differential Common-Mode Voltage Range	V_{CM}	Include V_{DI}	0.8		2.5	V
Single-Ended Input-Low Voltage	V_{IL}				0.8	V
Single-Ended Input-High Voltage	V_{IH}		2.0			V
Hysteresis	V_{HYS}			250		mV
Output Voltage Low	V_{OL}	R_L = 1.5kΩ from D+ or D- to 3.6V			0.3	V
Output Voltage High	V_{OH}	R_L = 15kΩ to GND	2.8		3.6	V
Off-State Leakage Current		Three-state driver	-1		+1	µA
Transceiver Capacitance	C_{IND}	D_ to GND		20		pF
Driver Output Impedance	R_{OUT}		2		15	Ω
ESD PROTECTION (D+, D-)						
Human Body Model				±15		kV
IEC 61000-4-2 Contact Discharge				±8		kV

TIMING CHARACTERISTICS

(V_{CC} = +4V to +5.5V, V_L = +1.6V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +2.5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER CHARACTERISTICS (C_L = 50pF)						
Rise Time D+/D-	t_{FR}	10% to 90% of $\lvert V_{OH}-V_{OL}\rvert$ (Figures 1, 9)	4		20	ns
Fall Time D+/D-	t_{FF}	90% to 10% of $\lvert V_{OH}-V_{OL}\rvert$ (Figures 1, 9)	4		20	ns
Rise- and Fall-Time Matching	t_{FR}/t_{FF}	Excluding the first transition from idle state, (Figure 1) (Note 2)	90		110	%

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TIMING CHARACTERISTICS (continued)

(V_{CC} = +4V to +5.5V, V_L = +1.6V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +2.5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Signal Crossover Voltage	V_{CRS}	(Figure 2) (Note 2)	1.3		2	V
Driver Propagation Delay	t_{PLH_DRV}	Low-to-high transition (Figure 2)			18	ns
	t_{PHL_DRV}	High-to-low transition (Figure 2)			18	ns
Driver-Enabled Delay Time	t_{PZH_DRV}	Off-to-high transition (Figures 3, 10)			20	ns
	t_{PZL_DRV}	Off-to-low transition (Figures 3, 10)			20	ns
Driver Disabled Delay	t_{PHZ_DRV}	High-to-off transition (Figures 3, 10)			20	ns
	t_{PLZ_DRV}	Low-to-off transition (Figures 3, 10)			20	ns
RECEIVER (C_L = 15pF)						
Differential Receiver Propagation Delay	t_{PLH_RCV}	Low-to-high transition (Figures 4, 9)			20	ns
	t_{PHL_RCV}	High-to-low transition (Figures 4, 9)			20	
Single-Ended Receiver Propagation Delay	t_{PLH_SE}	Low-to-high transition (Figures 4, 9)			12	ns
	t_{PHL_SE}	High-to-low transition (Figures 4, 9)			12	
Single-Ended Receiver Disable Delay	t_{PHZ_SE}	High-to-off transition (Figure 5)			15	ns
	t_{PLZ_SE}	Off-to-low transition (Figure 5)			15	
Single-Ended Receiver Enable Delay	t_{PZH_SE}	Off-to-high transition (Figure 5)			15	ns
	t_{PZL_SE}	Off-to-low transition (Figure 5)			15	

Note 1: Parameters are 100% production tested at +25°C, unless otherwise noted. Limits over temperature are guaranteed by design.

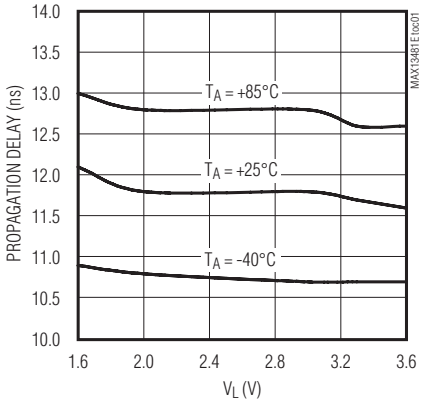
Note 2: Guaranteed by design, not production tested.

Note 3: Including external 27Ω series resistor.

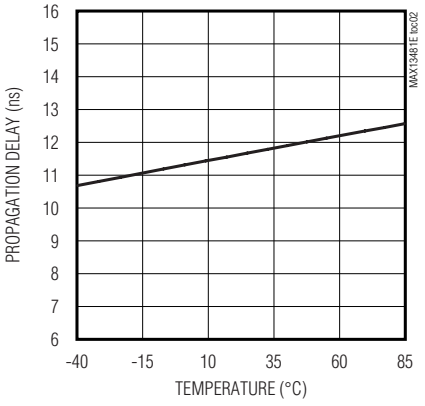
Typical Operating Characteristics

(V_{BUS} = 5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

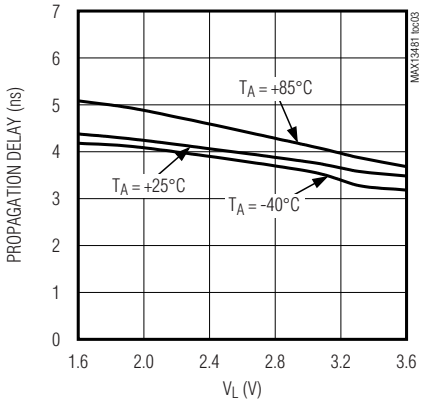
DIFFERENTIAL RECEIVER PROPAGATION DELAY vs. V_L



DIFFERENTIAL RECEIVER PROPAGATION DELAY vs. TEMPERATURE



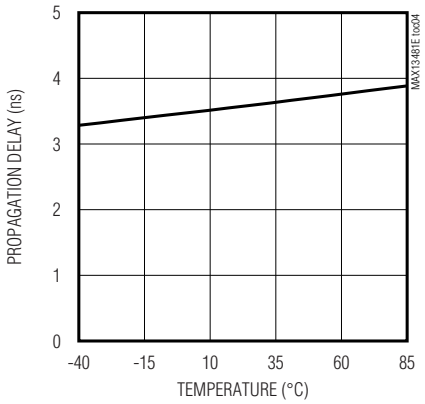
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_L



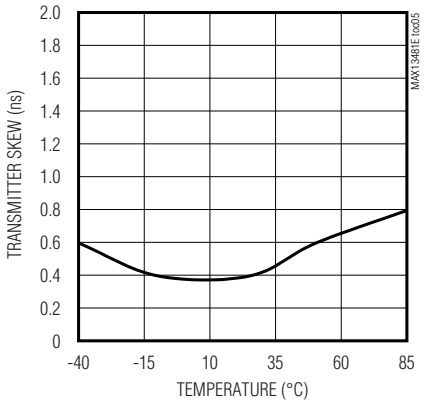
Typical Operating Characteristics (continued)

(V_{BUS} = 5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

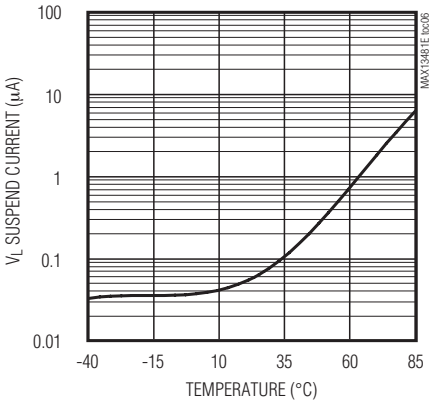
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. TEMPERATURE



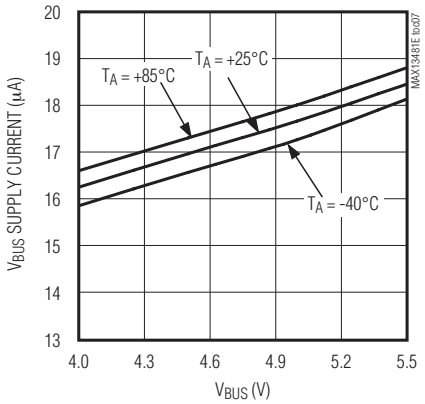
TRANSMITTER SKEW vs. TEMPERATURE



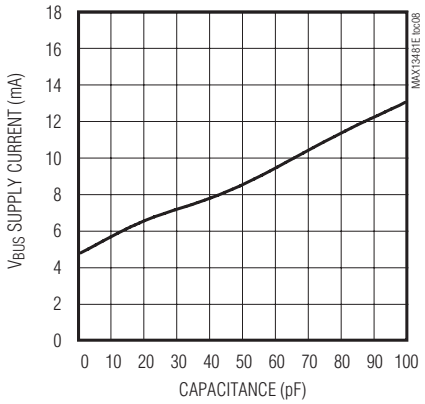
V_L SUSPEND CURRENT vs. TEMPERATURE



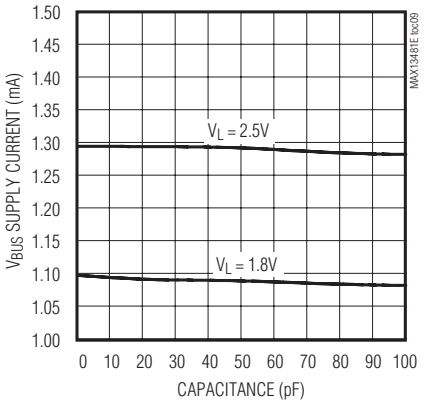
V_{BUS} SUSPEND CURRENT vs. V_{BUS}



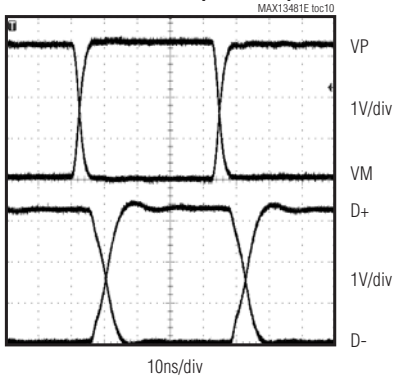
V_{BUS} SUPPLY CURRENT vs. D+/D- CAPACITANCE



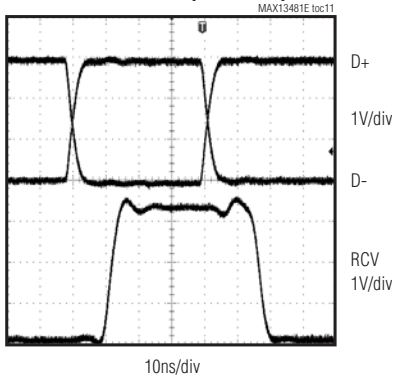
V_L SUPPLY CURRENT vs. D+/D- CAPACITANCE



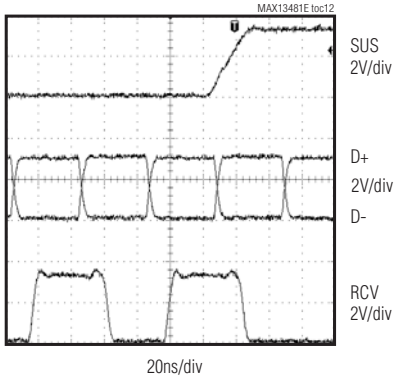
TRANSMIT MODE ($\overline{OE}$ = LOW)



RECEIVE MODE ($\overline{OE}$ = HIGH)



SUSPEND MODE

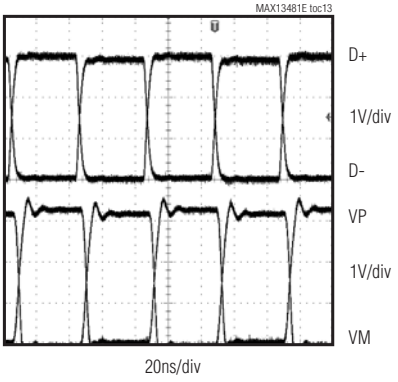


±15kV ESD-Protected USB Transceivers with External/Internal Pullup Resistors

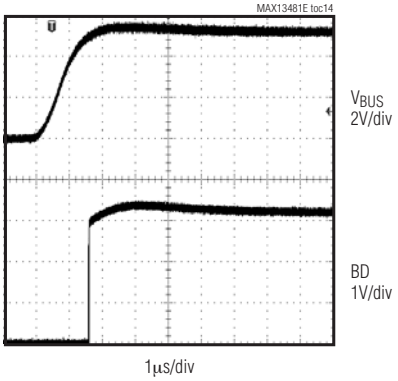
Typical Operating Characteristics (continued)

(V_{BUS} = 5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

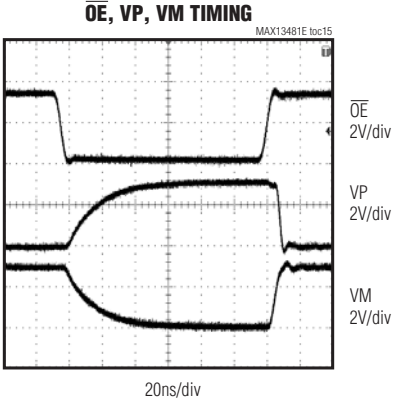
TRANSMISSION IN SUSPEND MODE



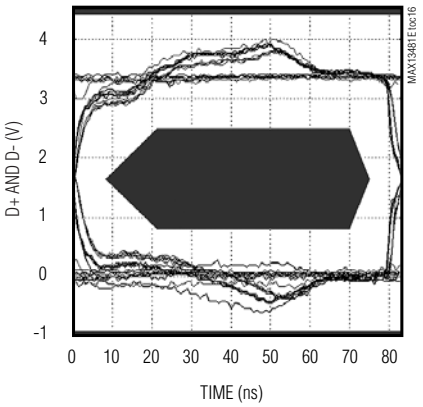
BUS DETECT RESPONSE



$\overline{OE}$, VP, VM TIMING



EYE DIAGRAM



Pin Description

PIN			NAME	FUNCTION
MAX13481E	MAX13482E	MAX13483E		
8, 16	1, 8	1, 5, 8	N.C.	No Connection. Not internally connected.
1	—	—	SP	Connect to V_L for Pin Compatibility to the MIC2551A or Leave Floating. Not internally connected.
2	2	2	RCV	Differential Receiver Output. RCV responds to the differential input on D+ and D-. RCV asserts low when SUS = V_L.
3	3	3	VP	Receiver Output/Driver Input. VP functions as a receiver output when $\overline{OE}$ = V_L. VP duplicates D+ when receiving. VP functions as a driver input when $\overline{OE}$ = GND.

Pin Description (continued)

PIN			NAME	FUNCTION
4	4	4	VM	Receiver Output/Driver Input. VM functions as a receiver output when $\overline{OE}$ = V_L. VM duplicates D- when receiving. VM functions as a driver input when $\overline{OE}$ = GND.
5	5	—	$\overline{ENUM}$	Active-Low Enumerator-Function-Selection Input. $\overline{ENUM}$ controls the pullup resistor or switch connection. See the *$\overline{ENUM}$* section.
6	6	6	GND	Ground
7	7	7	SUS	Suspend Input. Drive SUS low for normal operation. Drive SUS high for low-power state. RCV asserts low and D+/ D- are high impedance in suspend mode. VP and VM remain active in suspend mode.
9	9	9	$\overline{OE}$	Output Enable. Drive $\overline{OE}$ to GND to enable the D+/D- transmitter outputs. Drive $\overline{OE}$ to V_L to disable the transmitter outputs. $\overline{OE}$ also controls the I/O directions of VP and VM (see Tables 3 and 4).
10	10	10	D-	USB Input/Output. For $\overline{OE}$ = GND, D- functions as a USB output with VM providing the input signal. For $\overline{OE}$ = V_L, D- functions as a USB input with VM functioning as a single-ended receiver output.
11	11	11	D+	USB Input/Output. For $\overline{OE}$ = GND, D+ functions as a USB output with VP providing the input signal. For $\overline{OE}$ = V_L, D+ functions as a USB input with VP functioning as a single-ended receiver output.
12	12	12	V_{TRM}	Regulated Output Voltage. V_{TRM} provides a 3.3V output derived from V_{BUS}. Bypass V_{TRM} to GND with a 1µF (min) low-ESR capacitor such as ceramic or plastic film types. V_{TRM} provides power to internal circuitry, the internal D+ pullup resistor, VPU and VPUR. Do not use V_{TRM} to power external circuitry.
13	—	—	VPU	Pullup Voltage. For $\overline{ENUM}$ = GND, VPU is pulled to an internal 3.3V voltage. Connect a 1.5kΩ resistor between D+ and VPU for full-speed operation. For $\overline{ENUM}$ = V_L, VPU is high impedance.
—	—	13	I.C.	Internally Connected. Leave open. Do not connect to external circuitry.
—	13	—	VPUR	Internal Pullup Resistor. VPUR is pulled to an internal 3.3V voltage through a 1.5kΩ resistor ($\overline{ENUM}$ = GND). Connect VPUR to D+ for full-speed operation. For $\overline{ENUM}$ = V_L, VPU is high impedance.
14	14	14	V_{BUS}	USB-Side Power-Supply Input. Connect a +4V to +5.5V power supply to V_{BUS}. V_{BUS} supplies power to the internal regulator. Bypass V_{BUS} to GND with a 1µF ceramic capacitor. Connect V_{BUS} and V_{TRM} together when powering the MAX13481E/MAX13482E/MAX13483E with an external power supply.
15	15	15	V_L	Digital Input/Output Connection Logic Supply. Connect a +1.6V to +3.6V supply to V_L. Bypass V_L to GND with a 0.1µF (min) low-ESR ceramic capacitor.
—	16	16	BD	USB Detector Output (Push/Pull). A high at BD signals to the ASIC that V_{BUS} is present.
EP	EP	EP	EP	Exposed Paddle. Connect EP to GND.

±15kV ESD-Protected USB Transceivers with External/Internal Pullup Resistors

Detailed Description

The MAX13481E/MAX13482E/MAX13483E ±15kV ESD-protected USB-compliant transceivers convert single-ended or differential logic-level signals to USB signals, and USB signals to single-ended or differential logic signals. These devices fully comply to USB 2.0 when operating at full-speed (12Mbps), and operate with V_L as low as 1.6V, ensuring compatibility with low-voltage ASICs. Integrated ±15kV ESD-circuitry protection protects D+ and D- bus connections.

The MAX13481E/MAX13483E require an external 1.5kΩ pullup resistor to V_{TRM} for full-speed operation. The MAX13481E requires an external 1.5kΩ pullup resistor and feature an active-low enumeration function that connects a +3.3V voltage at VPU. The MAX13482E features an active-low enumeration function that connects a 1.5kΩ pullup resistor at VPUR for full-speed operation. The MAX13482E/MAX13483E also provide a bus detect (BD) output that asserts high when V_{BUS} > 3.6V.

Applications Information

Power-Supply Configurations

Normal Operating Mode

Connect V_L and V_{BUS} to system power supplies (Table 1). Connect V_L to a +1.6V to +3.6V supply. Connect V_{BUS} to a +4.0V to +5.5V supply or to the V_{BUS} connector.

Alternatively, these parts can derive power from a single Li+ cell. Connect the battery to V_{BUS}. V_{TRM} remains above +3.0V for V_{BUS} as low as +3.1V. Additionally, the devices can be powered by an external +3.3V ±10% voltage regulator. Connect V_{BUS} and V_{TRM} to an external +3.3V voltage regulator. V_{BUS} no longer consumes current to power the internal linear regulator in this configuration. The bus detect function (BD) on the MAX13482E and MAX13483E does not function when the device is powered this way.

Disable Mode

Connect V_{BUS} to a system power supply and leave V_L unconnected or connect to GND. D+ and D- enter a tri-state mode and V_{BUS} (or V_{BUS} and V_{TRM}) consumes less than 20µA of supply current. D+ and D- withstand external signals up to +5.5V in disable mode (Table 2).

Table 1. Power-Supply Configuration

V_{BUS} (V)	V_{TRM} (V)	V_L (V)	CONFIGURATION	NOTES
+4.0 to +5.5	+3.0 to +3.6 output	+1.6 to +3.6	Normal mode	—
+4.0 to +5.5	+3.0 to +3.6 output	GND or floating	Disable mode	Table 2
GND or floating	High Z	+1.6 to +3.6	Sharing mode	Table 2
+3.1 to +4.5	+3.0 to +3.6 output	+1.6 to +3.6	Battery supply	—
+3.0 to +3.6	+3.0 to +3.6 input	+1.6 to +3.6	Voltage regulator supply	

Table 2. Disable-Mode and Sharing-Mode Connection

INPUTS/OUTPUTS	DISABLE MODE	SHARING MODE
V_{BUS} / V_{TRM}	4V to 5.5V	Floating or connected to GND
V_L	Floating or connected to GND	1.6V to 3.6V input
D+ and D-	High impedance	High impedance
VP and VM	Invalid*	For $\overline{OE}$ = low, high impedance
		For $\overline{OE}$ = high, output logic high
RCV	Invalid*	Undefined
BD (MAX13482E/MAX13483E)	Invalid*	Low

**High impedance or logic low*

Sharing Mode

Connect V_L to a system power supply and leave V_{BUS} (or V_{BUS} and V_{TRM}) unconnected or connect to GND. D+ and D- enter a tri-state mode, allowing other circuitry to share the USB D+ and D- lines. V_L consumes less than 20µA of supply current. D+ and D- withstand external signals up to +5.5V in sharing mode (Table 2).

Device Control

$\overline{OE}$

$\overline{OE}$ controls the direction of communication. Drive $\overline{OE}$ low to transfer data from the logic side to the USB side. For $\overline{OE}$ = low, VP and VM serve as differential driver inputs to the USB transmitter. Drive $\overline{OE}$ high to transfer data from the USB side to the logic side. For $\overline{OE}$ = high, VP and VM serve as single-ended receiver outputs from the USB inputs (D+ and D-). RCV serves as a differential receiver output, regardless of the state of $\overline{OE}$.

$\overline{ENUM}$ (MAX13481E/MAX13482E)

The MAX13481E/MAX13482E feature an active-low enumerate function that allows software control of the 1.5kΩ pullup resistor and switch to D+ for full-speed operation.

For the MAX13481E, connect a 1.5kΩ pullup resistor between D+ and VPU. The MAX13481E provides an internal switch that pulls VPU to a +3.3V voltage. Drive $\overline{ENUM}$ high to disconnect VPU from voltage. Drive $\overline{ENUM}$ low to connect VPU and the external pullup resistor to the +3.3V voltage.

The MAX13482E has an internal 1.5kΩ resistor that connects at VPUR. Connect VPUR directly to D+. Drive $\overline{ENUM}$ high to disconnect the internal pullup resistor at VPUR. Drive $\overline{ENUM}$ low to connect the internal pullup resistor to VPUR.

SUS

The SUS state determines whether the MAX13481E/MAX13482E/MAX13483E operate in normal mode or in suspend mode. Connect SUS to GND to enable normal operation. Drive SUS high to enable suspend mode. RCV asserts low and VP and VM remain active in suspend mode (Tables 3 and 4). In suspend mode, supply current is reduced.

Table 3. Transmit Truth Table ($\overline{OE}$ = 0)

INPUTS		OUTPUTS	
VP	VM	D+	D-
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Table 4a. Receive Truth Table ($\overline{OE}$ = 1)

INPUTS		OUTPUTS		
D+	D-	VP	VM	RCV
0	0	0	0	RCV*
0	1	0	1	0
1	0	1	0	1
1	1	1	1	X

* = Last state
X = Undefined

Table 4b. Receive Truth Table ($\overline{OE}$ = 1, SUS = 1)

INPUTS		OUTPUTS		
D+	D-	VP	VM	RCV
0	0	0	0	0
0	1	0	1	0
1	0	1	0	0
1	1	1	1	0

±15kV ESD-Protected USB Transceivers with External/Internal Pullup Resistors

V_{TRM}

An internal linear regulator generates the V_{TRM} voltage (+3.3V, typ). V_{TRM} derives power from V_{BUS} (see the *Power-Supply Configurations* section). V_{TRM} powers the internal portions of the USB circuitry and provides the pullup voltage for the MAX13481E/MAX13482E. Bypass V_{TRM} to GND with a 1µF ceramic capacitor as close to the device as possible. Do not use V_{TRM} to provide power to any other external circuitry.

D+ and D-

D+ and D- serve as bidirectional bus connections and are ESD-protected to ±15kV (Human Body Model). For $\overline{OE}$ = low, D+ and D- serve as transmitter outputs. For $\overline{OE}$ = high, D+ and D- serve as receiver inputs.

BD (MAX13482E/MAX13483E)

The push-pull bus detect (BD) output monitors V_{BUS} and asserts high if V_{BUS} is greater than V_{TH_H}. BD asserts low if V_{BUS} is less than V_{TH_L}, and the MAX13482E/MAX13483E enter sharing mode (Table 2).

V_{BUS}

For most applications, V_{BUS} connects to the V_{BUS} terminal on the USB connector (see the *Power-Supply Configurations* section). V_{BUS} can also connect to an external supply. Drive V_{BUS} low to enable sharing mode. Bypass V_{BUS} to GND with a 1µF ceramic capacitor as close to the device as possible.

External Components

External Capacitors

The MAX13481E/MAX13482E/MAX13483E require three external capacitors for proper operation. Bypass V_L to GND with a 0.1µF ceramic capacitor. Bypass V_{BUS} to GND with a 1µF ceramic capacitor. Bypass V_{TRM} to GND with a 1µF (min) ceramic capacitor. Install all capacitors as close to the device as possible.

External Resistor

Proper USB operation requires two external resistors, each 27Ω ±1%. Install one resistor in series between D+ of the MAX13481E/MAX13482E/MAX13483E and D+ on the USB connector. Install the other resistor in series between D- of the MAX13481E/MAX13482E/MAX13483E and D- on the USB connector (see the *Typical Operating Circuits*). The MAX13483E requires an external 1.5kΩ pullup resistor between V_{TRM} and D+ for full-speed operation. The MAX13481E requires an external 1.5kΩ pullup resistor between VPU and D+ for full-speed operation. The MAX13482E does not require an external pullup resistor but VPUR must be connected to D+ for full-speed operation.

Data Transfer

Transmitting Data to the USB

To transmit data to the USB, drive $\overline{OE}$ low. The MAX13481E/MAX13482E/MAX13483E transmit data to the USB differentially on D+ and D-. VP and VM serve as input signals to the differential driver and are also used to assert a single-ended zero (SE0) driver (see Table 3).

Receiving Data from the USB

To receive data from the USB, drive $\overline{OE}$ high and SUS low. Differential data received by D+ and D- appears at RCV. Single-ended receivers on D+ and D- drive VP and VM, respectively.

RCV

RCV monitors D+ and D- when receiving data. RCV is a logic 1 for D+ high and D- low. RCV is a logic 0 for D+ low and D- high. RCV retains its last valid state when D+ and D- are both low (single-ended zero, or SE0).

ESD Protection

D+ and D- possess extra protection against static electricity to protect the devices up to ±15kV. The ESD structures withstand high ESD in all operating modes: normal operation, suspend mode, and powered down. D+ and D- provide protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge method specified in IEC 61000-4-2
- To protect V_{BUS} from ±15kV ESD, a 1µF or greater capacitor must be connected from V_{BUS} to GND.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 6 shows the Human Body Model and Figure 7 shows the current waveform generated when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which then discharges into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2, due to lower series resistance. Hence, the ESD with-

Timing Diagrams

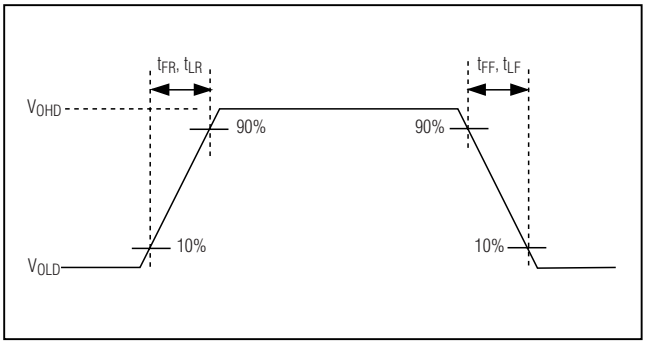


Figure 1. Rise and Fall Times

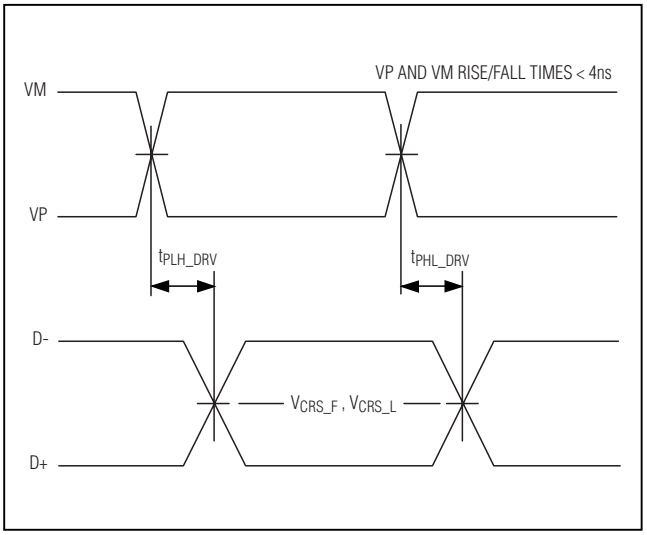


Figure 2. Timing of VP and VM to D+ and D-

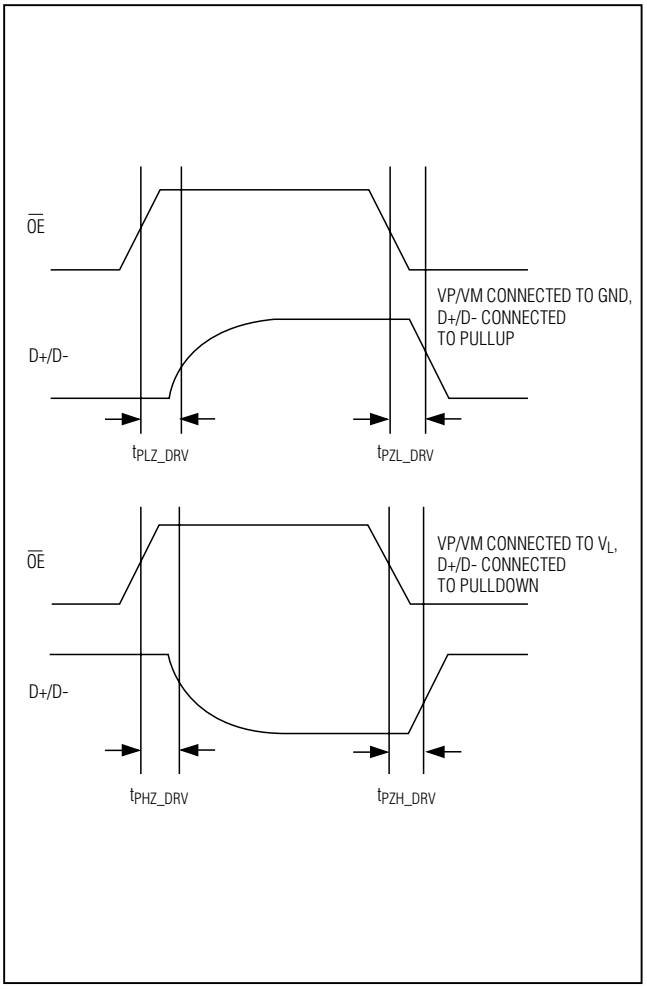


Figure 3. Driver's Enable and Disable Timing

stand voltage measured to IEC 61000-4-2 generally is lower than that measured using the Human Body Model. Figure 8 shows the IEC 61000-4-2 model. The Contact Discharge method connects the probe to the device before the probe is charged.

Machine Model

The Machine Model for ESD tests all connections using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. All pins require this protection during manufacturing, not just inputs and outputs. After PC board assembly, the Machine Model is less relevant to I/O ports.

±15kV ESD-Protected USB Transceivers with External/Internal Pullup Resistors

Timing Diagrams (continued)

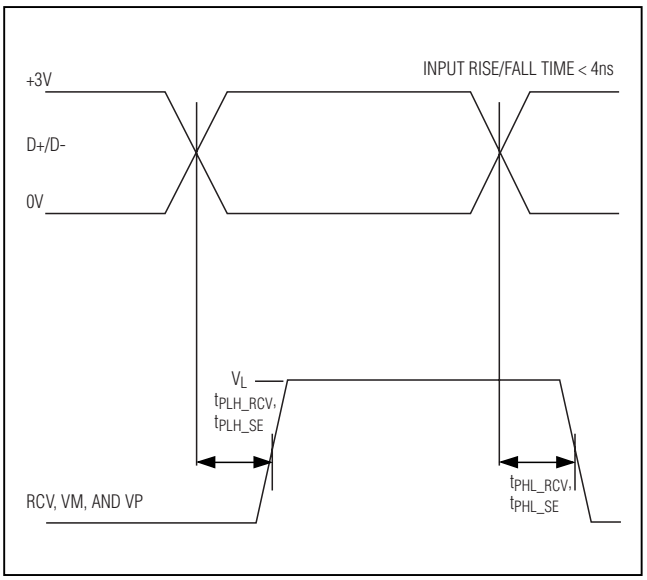


Figure 4. D+/D- Timing to VP, VM, and RCV

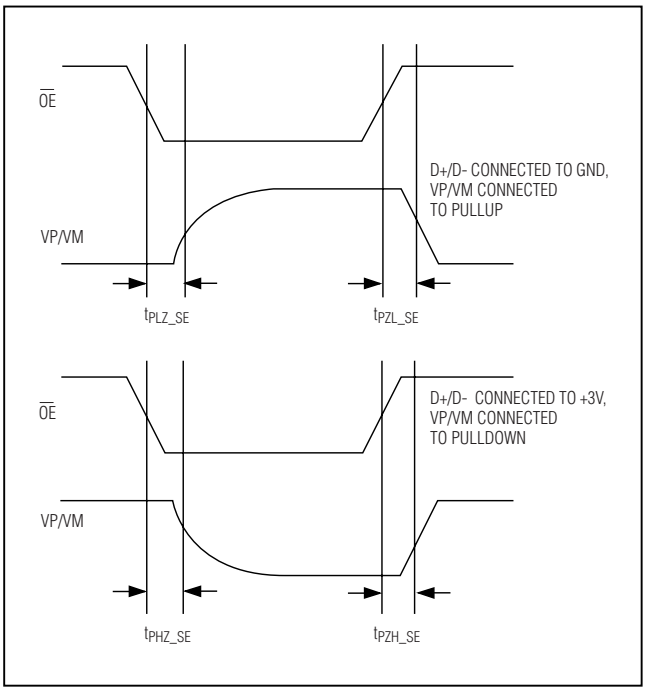


Figure 5. Receiver's Enable and Disable Timing

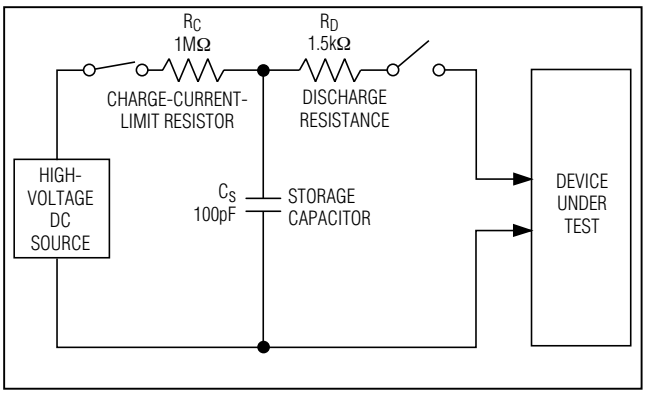


Figure 6. Human Body ESD Test Model

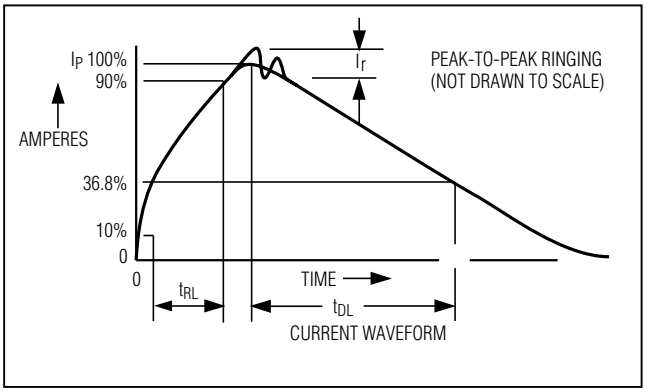


Figure 7. Human Body Model Current Waveform

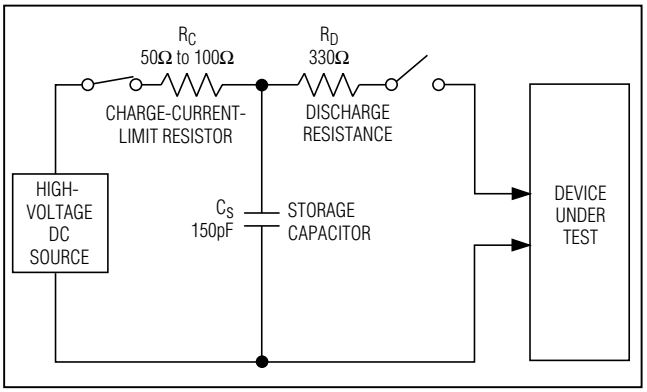


Figure 8. IEC 61000-4-2 ESD Test Model

Test Circuits

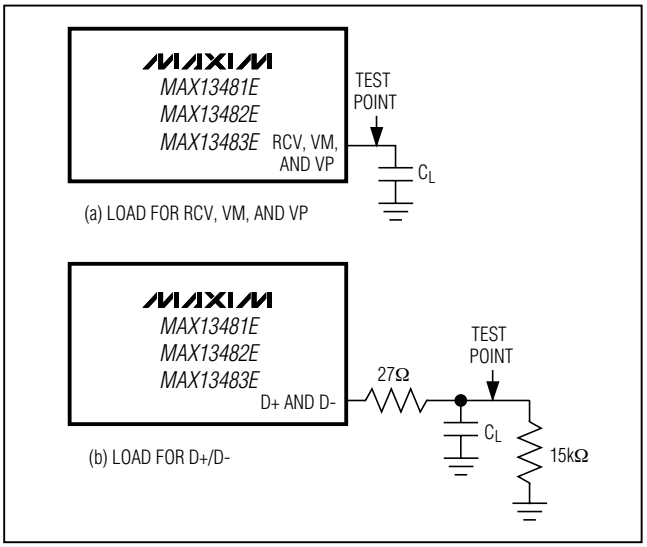


Figure 9. Transmitter and Receiver Propagation Delay

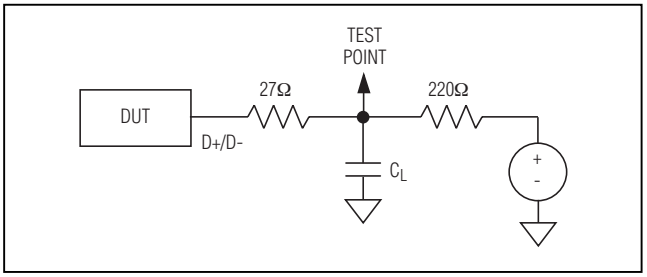
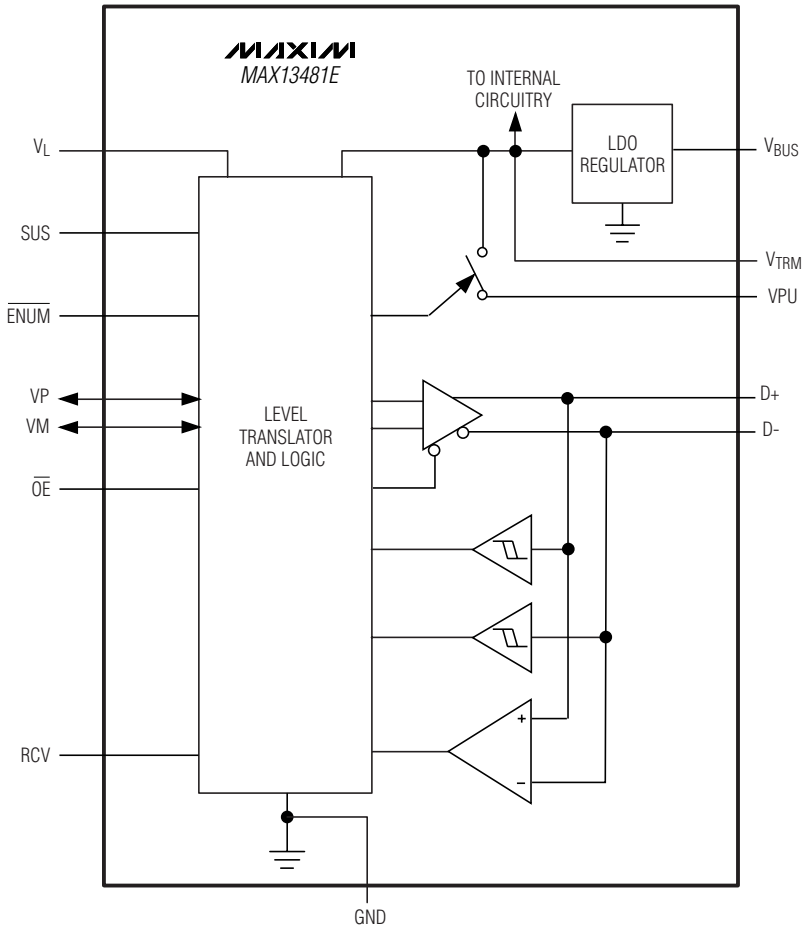
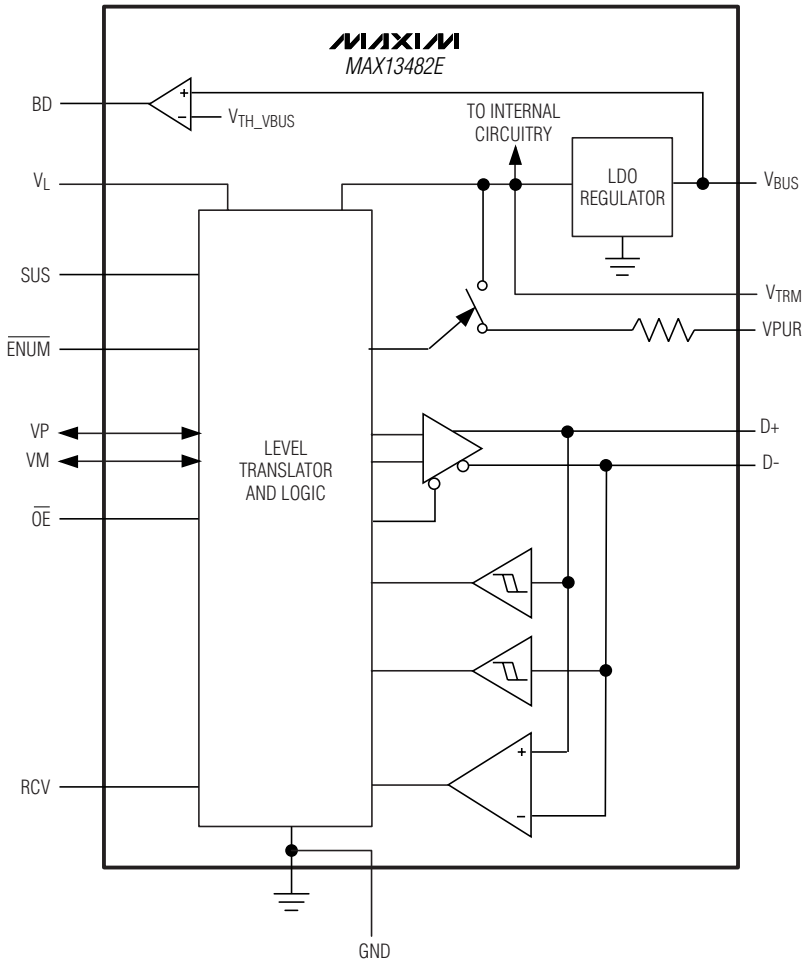


Figure 10. Driver's Enable and Disable Timing

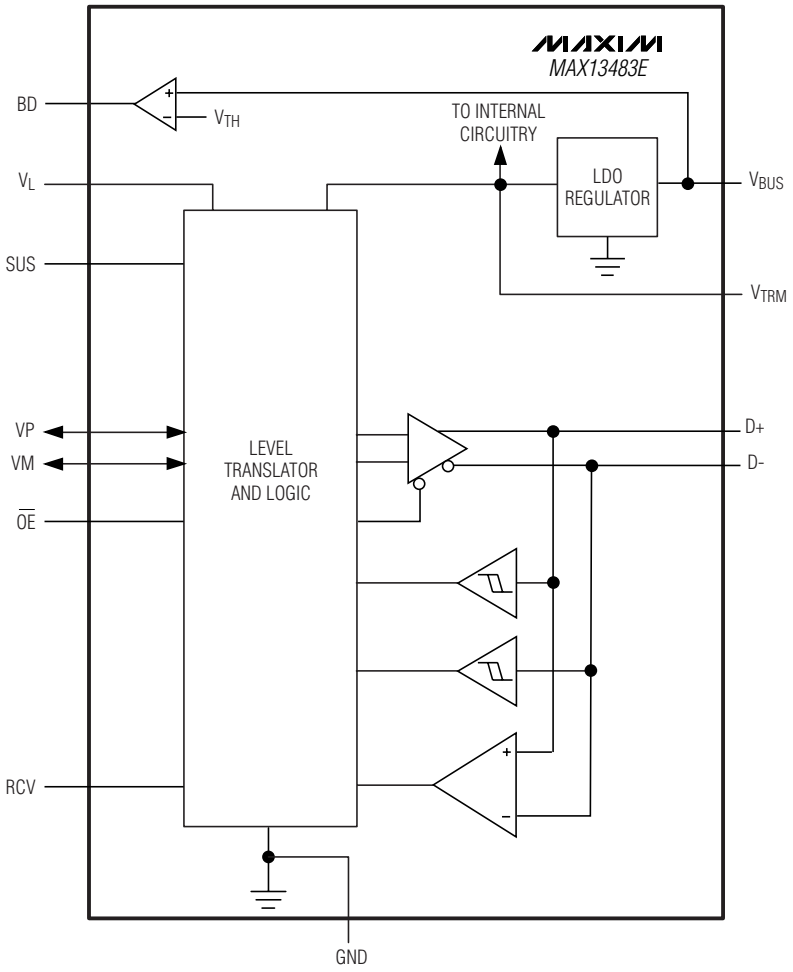
Functional Diagrams



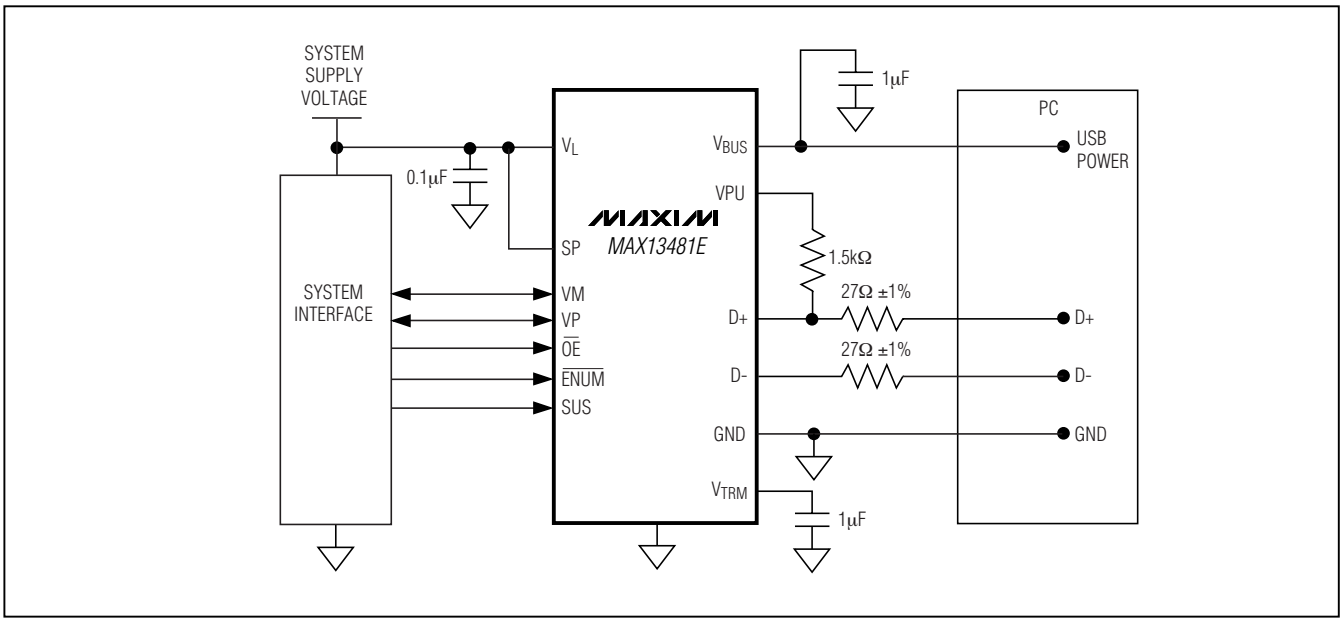
Functional Diagrams (continued)

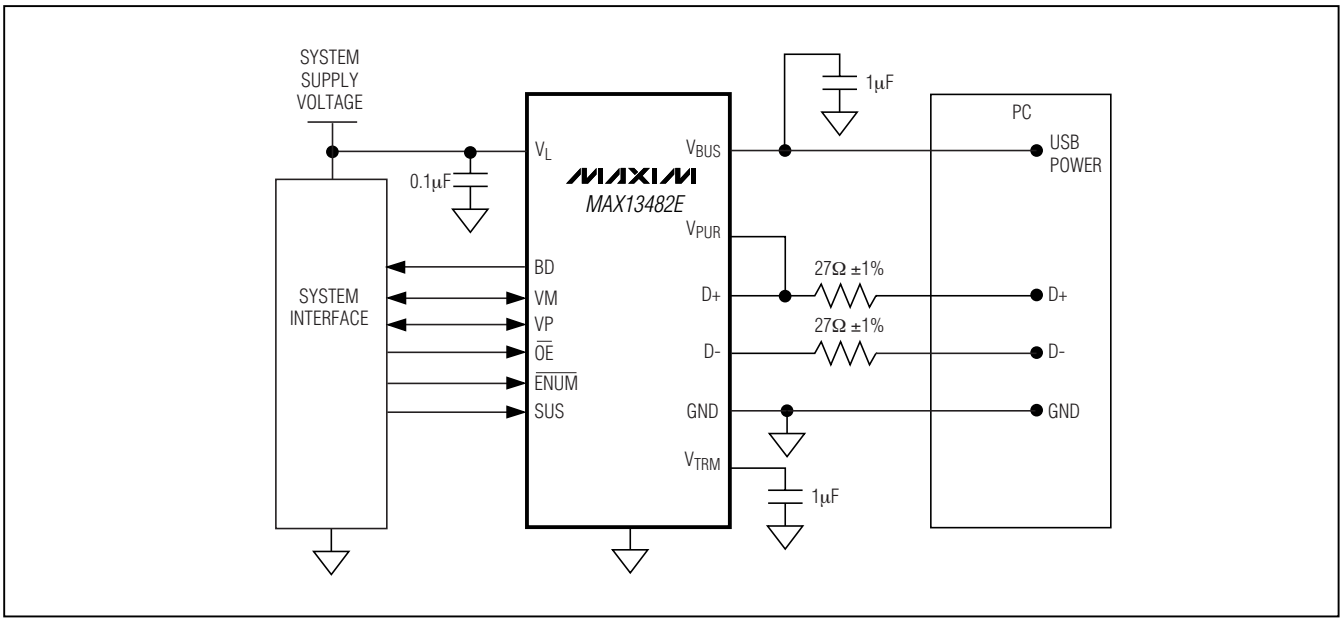


Functional Diagrams (continued)



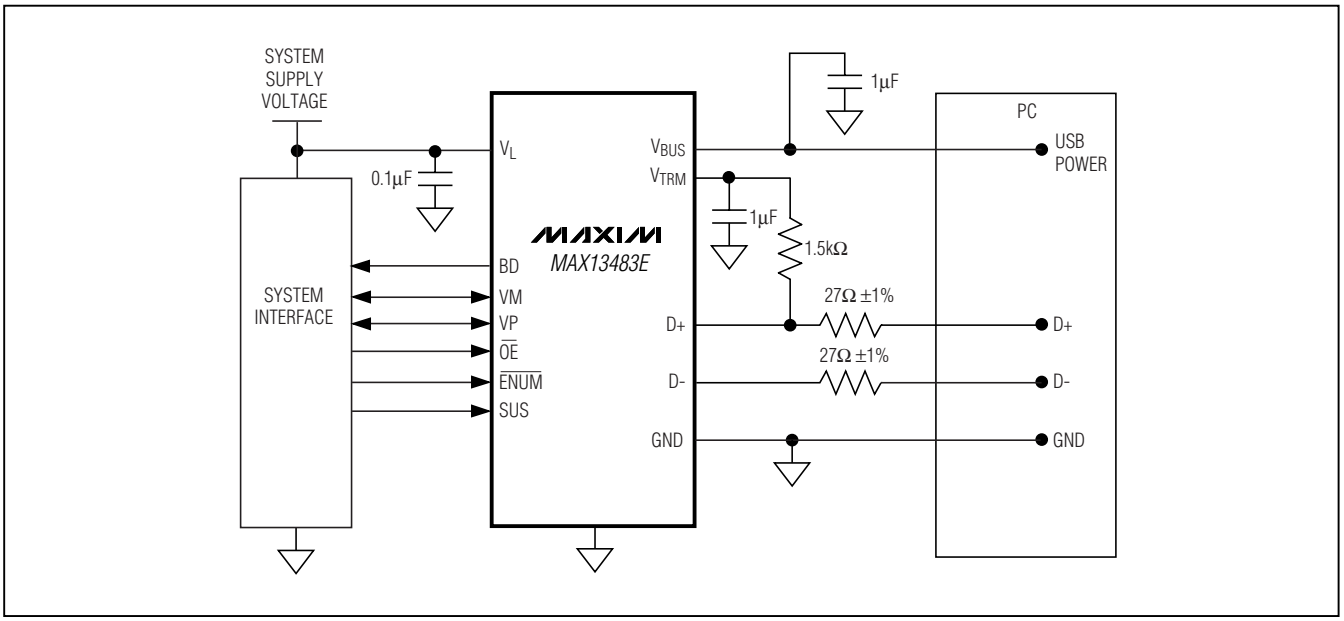
Typical Operating Circuits





±15kV ESD-Protected USB Transceivers with External/Internal Pullup Resistors

Typical Operating Circuits (continued)



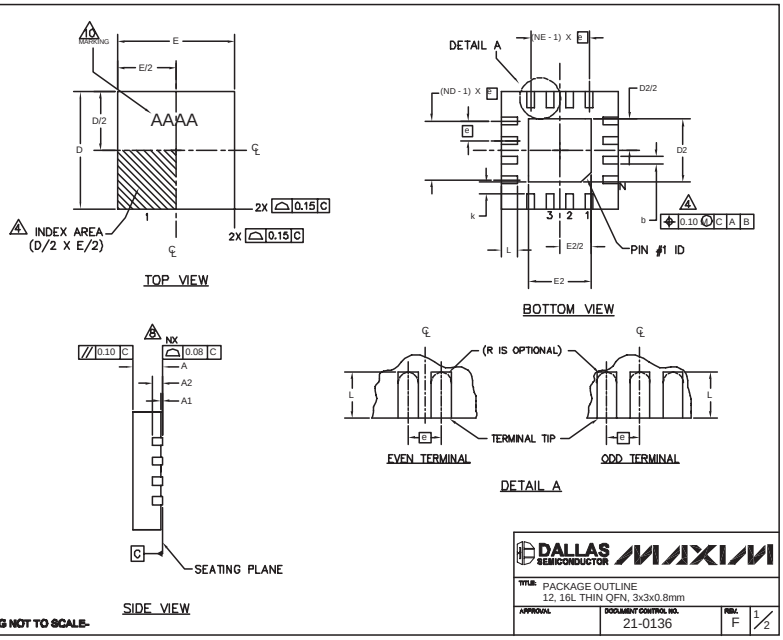
Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE 12, 16L THIN QFN, 3x3x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	F	1/2

PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE 12, 16L THIN QFN, 3x3x0.8

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	F	2/2

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